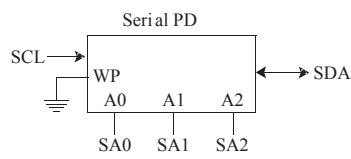
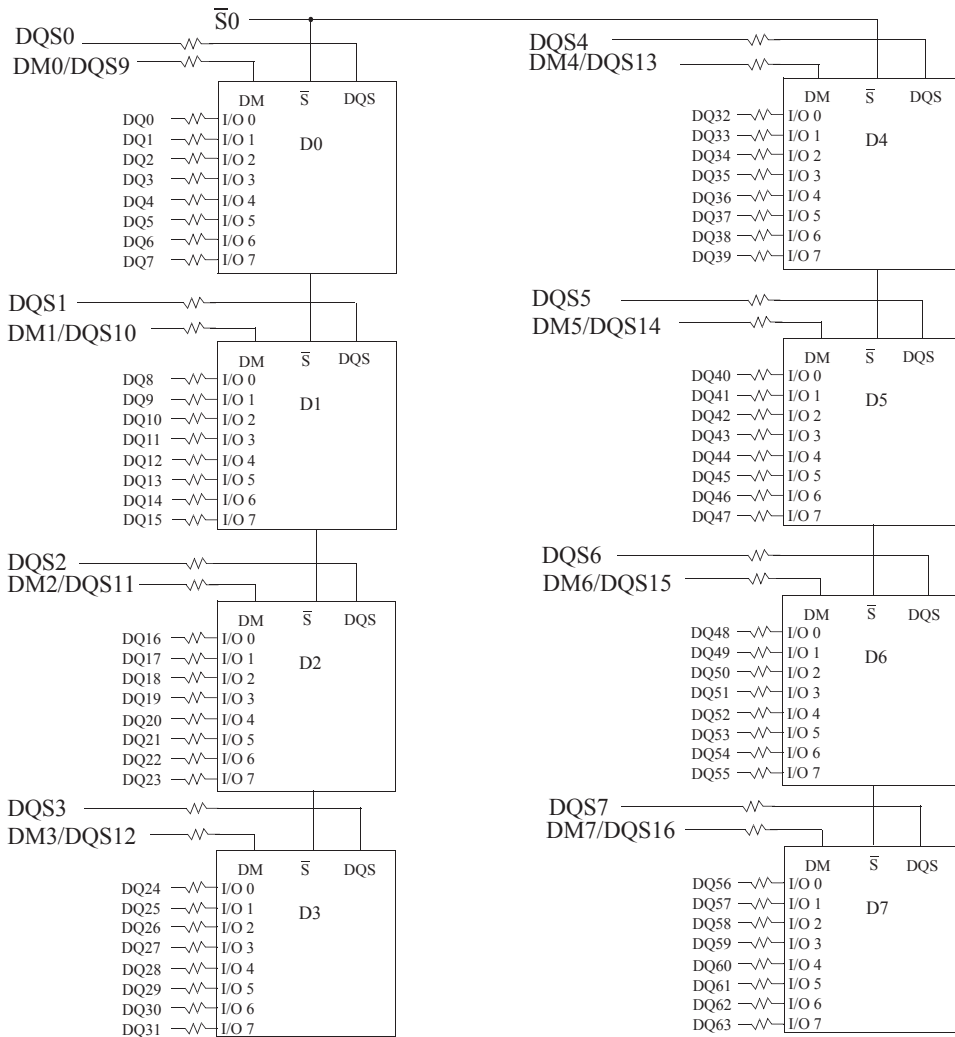


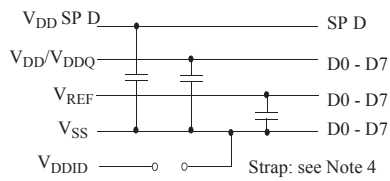
Functional Block Diagram



* Clock Wiring	
Clock Input	SDRAMs
*CK0/ $\overline{\text{CK0}}$	2 SDRAMs
*CK1/ $\overline{\text{CK1}}$	3 SDRAMs
*CK2/ $\overline{\text{CK2}}$	3 SDRAMs

* Wire per Clock Loading Table/ Wiring Diagrams

- BA0 - BA1 → BA0-BA1: SDRAMs D0 - D7
- A0 - A12 → A0-A12: SDRAMs D0 - D7
- $\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMs D0 - D7
- $\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMs D0 - D7
- CKE0 → CKE: SDRAMs D0 - D7
- $\overline{\text{WE}}$ → $\overline{\text{WE}}$: SDRAMs D0 - D7



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE /S relationship must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms \pm 5%
4. V_{DDID} strap connections (for memory device V_{DD} , V_{DDQ}):
STRAP OUT (OPEN): $V_{\text{DD}} = V_{\text{DDQ}}$
STRAP IN (V_{SS}): $V_{\text{DD}} \neq V_{\text{DDQ}}$
5. BAx, Ax, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ resistors: 5.1 ohms \pm 5% (Except PC2100)