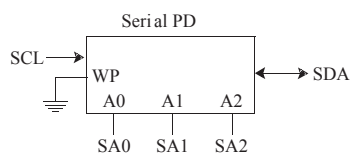
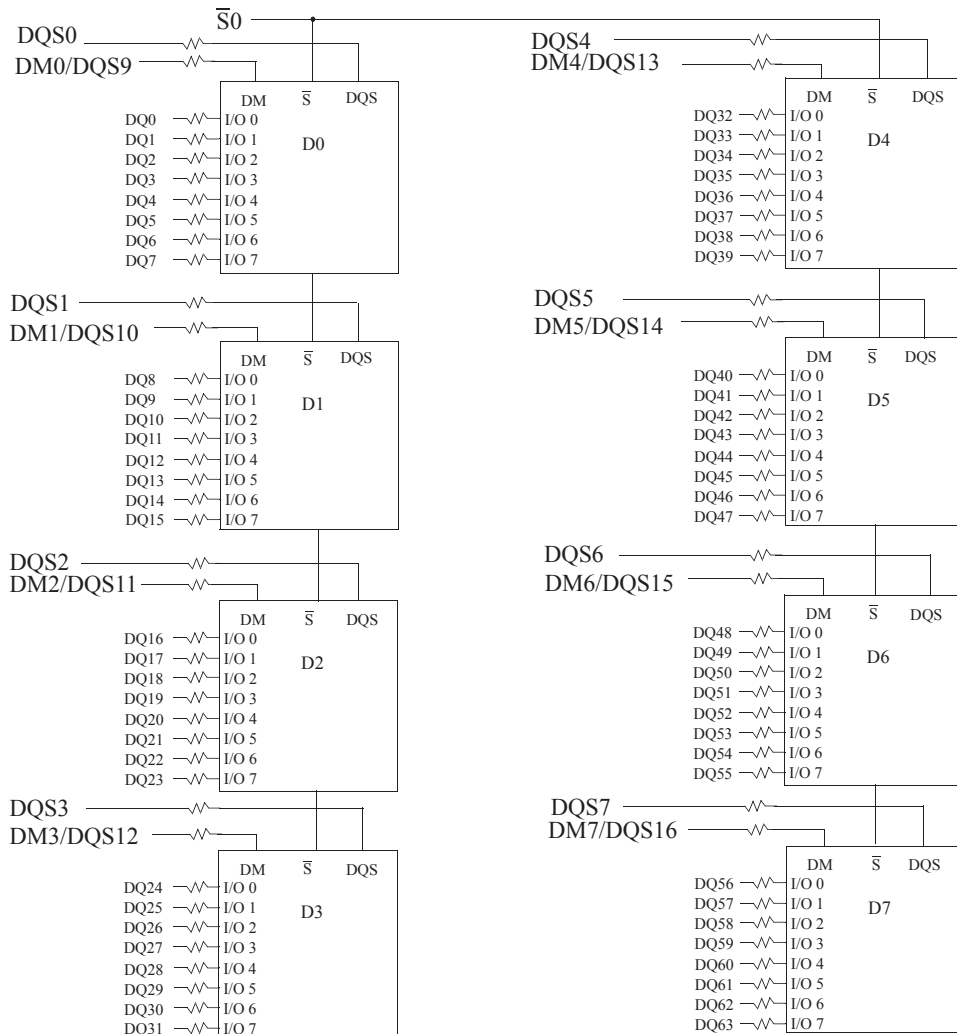


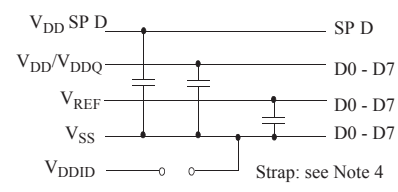
Functional Block Diagram



* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	2 SDAMs
*CK1/CK1	3 SDAMs
*CK2/CK2	3 SDAMs

* Wire per Clock Loading Table/ Wiring Diagrams

- BA0 - BA1 → BA0-BA1: SDRAMs D0 - D7
- A0 - A12 → A0-A12: SDRAMs D0 - D7
- \overline{RAS} → \overline{RAS} : SDRAMs D0 - D7
- \overline{CAS} → \overline{CAS} : SDRAMs D0 - D7
- CKE0 → CKE: SDRAMs D0 - D7
- \overline{WE} → \overline{WE} : SDRAMs D0 - D7



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE /S r relationship must be maintained as shown.
3. DQ, DQS, DM/DQS resistor s: 22 oh ms ± 5%
4. V_{DDID} strap connections (for memo ry device V_{DD}, V_{DDQ}): STRAP OUT (OPEN): V_{DD} = V_{DDQ} STRAP IN (V_{SS}): V_{DD} ≠ V_{DDQ}.
5. BA_x, A_x, \overline{RAS} , \overline{CAS} , \overline{WE} resistors: 5.1 ohms ±5% (Except PC2100)